

DATA 620-I



DATA MACHINES
Division of DECISION Control, Inc.

DATA/620•I

INTRODUCTION

DATA/620 I, shown in actual size on the cover, is a system oriented digital computer. It occupies only 10½" of a 19" x 24" relay rack, weighs less than 100 lbs., and requires only 350 watts. Developed for operation with other electronic devices performing information and control functions automatically. Features integrated circuit high reliability, interfacing ease, I/O balanced with processing power, over 100 commands, and hardware registers for arithmetic and addressing speed. Fully supported with field proven existing software, programming and maintenance training, peripheral equipment, and interfacing hardware.

DATA/620 I is modular in concept to economically match the tasks to be performed. The Processor can be supplied with memories ranging from 1024 to 32,768 words of 16 or 18 bits. A single small task to be performed automatically easily justifies the low cost of the DATA/620 I, although numerous large tasks won't saturate the processing and throughput power. Uncomplicated and trustworthy enough to be put into a system and be forgotten. Flexible and economic enough to replace special purpose electronic control systems. Safe enough to let very expensive processes depend on DATA/620 I performance.

DATA/620 I is an emphasis of cost cutting techniques to produce an "end" solution at the lowest possible cost. 620 I prices are low, interfacing costs are low, service costs negligible. All DATA/620 field proven software operates on DATA/620 I, making the solution programming easy and economical. Complementary I/O peripheral devices are attractively priced. The pricing offers new opportunities of cost savings and solution approaches to the system designer, product planner, development engineer and, most of all, to the end USER.

TYPICAL PRICES!

DATA/620 I processor	\$ 6,000
4096 x 16 bit memory	\$ 6,500
16,768 x 16 bit memory	\$23,000
ASR 33 TTY	\$ 1,400

FEATURES

SILICON MONOLITHIC INTEGRATED CIRCUITS
NINE HARDWARE REGISTERS
107 BASIC COMMANDS
SIX ADDRESSING MODES
DIRECT ADDRESSING TO 2048 OR 32,768
16 OR 18 BIT WORDS
EXPANSION TO 32,768 WORDS
HARDWARE INDEX REGISTERS
PARTY LINE I/O FACILITY
MICRO-EXEC OPTION
10½" OF RACK SPACE
LESS THAN 90 LBS.
340 WATTS
NPN AND PNP I/O LEVELS
PLUG-IN EXPANDABLE
FIELD PROVEN SOFTWARE
COMPATIBLE WITH DATA 620
PORTABLE



SPECIFICATIONS

TYPE	A system Computer, general purpose digital, designed for on-line data systems, magnetic core memory, binary, parallel, single-address, with bus organization and micro-control.	
MEMORY	Magnetic Core, 16 or 18 bits, 1.8 microseconds full cycle, 700 nanoseconds access time, 1024 words minimum expandable to 32,768 words. Each module with data and address register.	
ARITHMETIC	Parallel, binary, fixed point, 2's complement.	
WORD LENGTH	16 or 18 bits.	
SPEED (FETCH & EXECUTE)	Add or Subtract	3.6 microseconds
	Multiply (optional)	18.0 microseconds, 16 bit 19.8 microseconds, 18 bit
	Divide (optional)	18.0 to 25 microseconds, 16 bit 19.8 to 28.8 microseconds, 18 bit
	Register change class	1.8 microseconds
	Input/Output— from A or B	3.6 microseconds
	from memory	5.4 microseconds
CONTROL	ADDRESSING MODES Direct addressing to 2048 words Relative to P register 512 words Index with X-register, hardware, does not add to execution time Index with B-register, hardware, does not add to execution time Multi-level indirect addressing Immediate Extended addressing (optional) INSTRUCTION TYPES Single word Generic Double word Micro-command	
	INSTRUCTIONS: 107 standard, and over 128 macro instructions.	
	Number	Type Time/Cycles
	3	Load 2
	3	Store 2
	5	Arithmetic (2 optional) Above
	3	Logical 2
	10	Jump 2
	10	Jump and Mark 2-3
	10	Execute 2
	14	Immediate (2 optional) 2
	13	Input/Output 1,2,3
	26	Register Change 1
	6	Logical Shift 1 + .25K
	6	Arithmetic Shift 1 + .25K
	2	Control 1
	14	Extended addressing (optional) 3
	Over 128 micro-instructions	
	MICRO-EXEC (Optional) Facility and hardware to construct a hardware program external to the DATA 620I. Eliminates stored program memory accessing by use of hardware program.	

OPERATION REGISTERS

BUFFER REGISTERS

INPUT/OUTPUT

PHYSICAL

Console

Display and data entry switches for all operational registers, 3 sense switches, instruction repeat, single step; run; power on/off.

A-register—accumulator, input/output, 16/18 bits.

B-register—double length accumulator, input/output, index register, 16/18 bits.

X-register—index register, 16/18 bits.

P-register—program counter, 16/18 bits.

R-register—operand register, 16/18 bits.

U-register—instruction register, 16/16 bits.

S-register—shift register, 5 bits, operates with the U-register for executing shift instructions.

L-register—memory address register, one L-register per memory module.

W-register—memory word register, 16/18 bits, one W-register per memory module.

Processor Input/Output Options

Programmed Data Transfer

Single word to/from memory

Single word to/from A and B registers

External control lines

External sense lines

Automatic Data Transfer

Direct memory access facility transfer with rates over 200,000 words per second.

Priority Interrupts

Group enable/disable, individually arm/disarm, single instruction interrupt capability.

Real-Time Clock

Adjustable time base: May be programmed as multiple internal timers.

Power Failure detect/restart

Interrupts on power failure and automatically restarts on power recovery.

DIMENSIONS

Main Frame (18 bits)—10½ inches high, 19 inches wide, 15 inches deep

WEIGHT

Main Frame 50 pounds

POWER

3 amps 115vac, 60hz (340 watts). 115 ± 10v, 60 ± 2hz.

Power supplies are regulated. Additional regulation is not required under normal commercial power sources.

EXPANSION

Main processor contains provisions and space for all internal options.

INSTALLATION

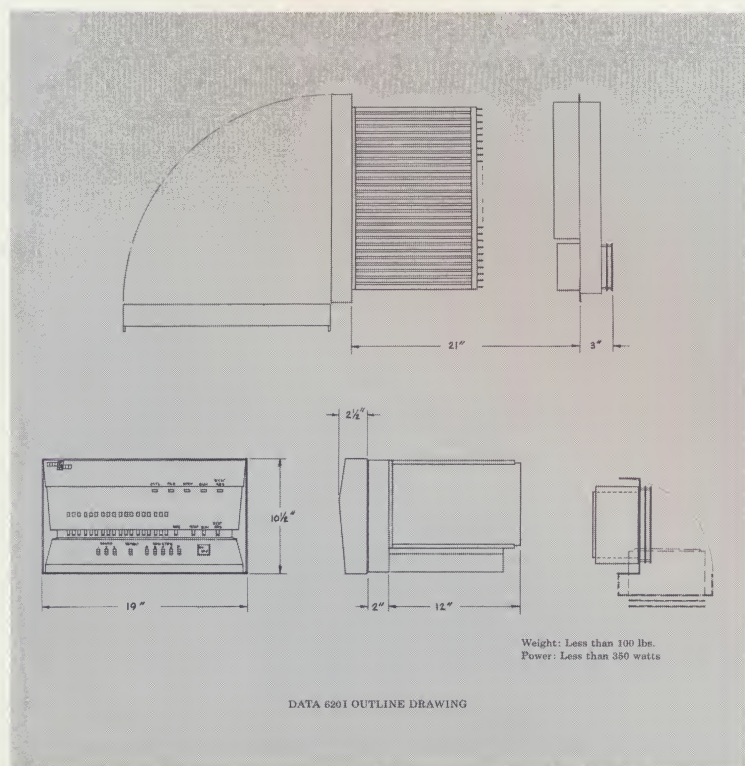
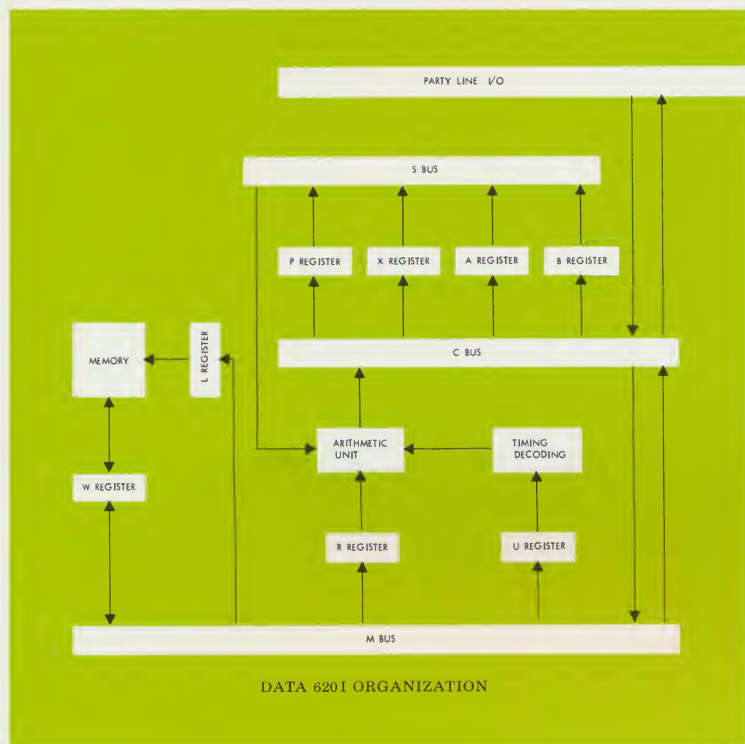
Mounts in standard 19 inch cabinet, no air conditioning, sub-flooring or special wiring and site preparation required.

ENVIRONMENTS

0°C to 45°C; 0 to 90% relative humidity.

MAINFRAME LOGIC AND SIGNALS

Integrated circuit, 2.2 mhz clock, logic levels 0v false, +5 true.



SYSTEM SOFTWARE

The programming aids provided with the DATA/620 I family were designed and developed with the principal objectives of maximizing user productivity and efficiency. These languages have been field-proven on the DATA/620 Computer. The programming languages and library subroutines conform to the most widely used standards and conventions. The software is modular in design such that user-oriented macros, pseudo operations, compiler statements, special hardware test routines and Input/Output drivers can be easily added. The documentation delivered with the system describes the construction and operation and contains a separate treatise describing how the user can add to or select a set of the standard software to enhance the effectiveness of the software for his particular application and system configuration. The major items of DATA/620 I software are listed below.

FORTRAN	LOGARITHMIC
DAS ASSEMBLER	EXPONENTIAL
AID	TRIGONOMETRIC
ON-LINE AID	CONVERSIONS
FLOATING POINT	I/O DRIVERS
MULTIPLE PRECISION	MAINTAIN EXEC.
CORRECT	VERIFY

PERIPHERAL EQUIPMENT

MAGNETIC TAPE TRANSPORTS — low speed 45 ips, medium speed 75 ips, high speed 120 ips. IBM standard formats with densities of 200, 556 or 800 bpi.

CARD EQUIPMENT — 85 cpm reader, 1,000 cpm reader, 100 cpm punch.

PRINTERS — High speed 1200 lpm, 12 columns; high speed 600 lpm, 120 columns; medium speed 300 lpm, 120 columns; low speed 10 cps KSR 33, KSR 35.

PAPER TAPE EQUIPMENT — Readers available in 300 cps or 10 cps, punches 60 cps, 120 cps or 10 cps.

MAGNETIC STORAGE DEVICE — Fixed head storage discs available in 65 K to 1/4 million words of storage. Average access time, 8.5 ms.

MISCELLANEOUS: Digital Plotters, Oscilloscope Display, Analog Input and Output, High and Low Level Assemblies, Data Set Couplers, Contact and Solid State Digital Units.

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DUREL advertising



OVF'L

PARITY

STEP

RESET

STEP

SENSE

2

3

REPEAT

REGISTER

A

B

X

U

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